

WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:
an insulating substrate;
a pair of first and second signal lines formed on the insulating substrate;
5 a third signal line formed on the insulating substrate and intersecting
the first and the second signal lines in an insulating manner;
a fourth signal line formed on the insulating substrate and intersecting
the second signal line in an insulating manner;
a pixel electrode formed in a pixel area defined by the intersections of
10 the first and the second signal lines and the third signal line and including a
plurality of subareas partitioned by cutouts;
a direction control electrode formed in the pixel area and including a
portion overlapping at least one of the cutouts;
a first thin film transistor connected to the pixel electrode, the first
15 signal line, and the third signal line;
a second thin film transistor connected to the pixel electrode, the second
signal line, and the third signal line; and
a third thin film transistor connected to the direction control electrode,
the second signal line, and the fourth signal line.
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2. The thin film transistor array panel of claim 1, wherein the fourth
signal line includes a portion overlapping at least one of the cutouts which does
not overlap the direction control electrode.
- 25 3. The thin film transistor array panel of claim 2, further
comprising a fifth signal line placed between the first and the second signal lines,
wherein the fourth signal line is located between the first and the second signal
lines and the fourth and the fifth signal lines have inversion symmetry.

4. The thin film transistor array panel of claim 1, wherein the fourth signal line is supplied with a common voltage.

5. The thin film transistor array panel of claim 1, wherein the cutouts comprise a transverse cutout bisecting the pixel electrode into upper and lower halves and a plurality of oblique cutouts having inversion symmetry with respect to the transverse cutout.

6. The thin film transistor array panel of claim 2, wherein the direction control electrode comprises substantially the same layer as the third signal line.